Day 1, Thursday, November 27

09:30–10:00  Registration and Coffee

10:00–10:10  MCC Opening

10:00–12:00  Session: Multicore and Cache
             Chair: Christoph Kessler
             1  Evaluation of CPU Hotplug Latency on Multi-Core ARM Chips: Simon Holmbacka and Johan Lilius
             2  Simulating a Manycore Processor: A Scalable Functional Model for the Adapteva Epiphany Architecture: Ola Jeppsson and Sally McKee
             3s  Modeling Performance Variation Due to Cache Sharing: Andreas Sembrant, Andreas Sandberg, David Black-Schaffer and Erik Hagersten
             4s  Undersubscribing Multi-Threaded Workloads on Clustered Cache Architectures: Wim Heirman, Trevor E. Carlson, Kenzo Van Craeynest, Ibrahim Hur, Aamer Jaleel and Lieven Eeckhout
             5s  A New Perspective for Efficient Virtual-Cache Coherence: Stefanos Kaxiras and Alberto Ros
             6s  Run time-Guided Cache Coherence Optimizations in Multi-core Architectures: Madhavan Manivannan and Per Stenström
             7s  SC²: A statistical compression cache scheme: Angelos Arelakis and Per Stenström

12:00–13:00  Lunch at Finn Inn

13:00–15:00  Session: GPU and Dataflow
             Chair: Krzysztof Kuchcinski
             Keynote: Massive Parallelism in Graphics Processors: Tomas Akenine-Möller (Intel and Lund University)
             8s  Performance-aware Global Composition Framework for GPU-based Systems: Usman Dastgeer and Christoph Kessler
             9s  Realizing Efficient Execution of Dataflow Actors on Manycores: Essayas Gebrewahid, Mingkun Yang, Gustav Cedersjö, Zain Ul-Abdin, Veronica Gaspes, Jörn W. Janneck and Bertil Svensson
             10s  An Evaluation of Code Generation of Dataflow Languages on Manycore Architectures: Suleyman Savas, Essayas Gebrewahid, Zain Ul-Abdin, Tomas Nordström and Mingkun Yang
             11s  The Multi-Resource Server for Predictable Execution on Multi-core Platforms: Rafia Inam, Nesredin Mahmud, Moris Behnam, Thomas Nolte and Mikael Sjödin
             Coffee break

15:30–17:00  Session: Memory and Energy
             Chair: Zain-ul-Abdin
             12  Validating Energy Compositionality of GPU Computations: Lu Li and Christoph Kessler
             13  Code Commentary and Automatic Refactorings using Feedback from Multiple Compilers: Nicklas Bo Jensen, Christian W. Probst and Sven Karlsson
             14s  Towards more efficient execution: a decoupled access-execute approach: Konstantinos Koukos, David Black-Schaffer, Vasileios Spiliopoulos and Stefanos Kaxiras
             15s  Performance and energy analysis of the restricted transactional memory implementation on haswell: Bhavishya Goel, Sally McKee, Per Stenström, Ruben Titos-Gil and Anurag Negi
             16s  A Runtime Manager for Gracefully Degrading SoCs: Stavros Tzilis and Ioannis Sourdis

16:30–17:15  Visit the Robotics Lab (group 1, register on next page) (partially overlaps the last session)

17:15–18:00  Visit the Robotics Lab (group 2, register on next page)

18:30–21:00  Conference dinner in Vattenhallen

All sessions are taking place in E-house, room E:1406
Day 2, Friday, November 28

9:00-10:00  Session: Runtime Support and Reconfigurability
  Chair: Flavius Gruian
  17 Blurring the Line: From Multicore Devices to the Internet of Things: Patrik Persson and Johan Eker
  18 Testing Infrastructure for Operating System Kernel Development: Maxwell Walter and Sven Karlsson
  19 Constraint Programming Approach to Reconfigurable Processor Extension Generation and Application Compilation: Kevin Martin, Christophe Wolinski, Krzysztof Kuchcinski, Antoine Floch and Francois Charot
  20 Evaluation of Level of Confidence and Optimization of Roll-back Recovery with Checkpointing for Real-Time Systems: Dimitar Nikolov and Erik Larsson
  Coffee break

10:30-12:00  Session: Data Structures
  Chair: Per Andersson
  21 The Effects of Granularity and Adaptivity on Private/Shared Classification for Coherence: Mahdad Davari, Alberto Ros, Erik Hagersten and Stefanos Kaxiras
  22 Enhancing Concurrent Data Structures with Concurrent Iteration Operations: Consistency Framework and Trade-offs: Yiannis Nikolakopoulos, Anders Gidenstam, Marina Papatriantafilou and Philippas Tsigas
  23 Performance and power consumption evaluation of concurrent queue implementations in embedded systems: Ivan Walulya, Lazaros Papadopoulos, Philippas Tsigas, Paul Renaud-Goud, Dimitrios Soudris and Brendan Barry
  24 Efficient lock-free binary search trees: Bapi Chatterjee, Nhan Nguyen and Philippas Tsigas

12:00–13:00  Lunch at Finn Inn

Posters
Displayed throughout the event, right outside the conference room, E:1406:
  25p Worst Case Delay Analysis of a DRAM Memory Request for COTS Multicore Architectures: Rafia Inam, Moris Behnam and Mikael Sjödin
  26p Trends in Static Power Consumption: Jörg Lenhardt, Wolfram Schiffmann and Jörg Keller
  27p Brief Announcement: Concurrent Data Structures for Efficient Streaming Aggregation: Daniel Cederman, Vincenzo Gulisano, Yiannis Nikolakopoulos, Marina Papatriantafilou and Philippas Tsigas
  28p Library Support for Resource Constrained Accelerators: Laust Brock-Nannestad and Sven Karlsson

Register for the Visit to The Robotics Lab
Please use this Doodle poll to register: [http://doodle.com/c9sr6vr8fomq3w3](http://doodle.com/c9sr6vr8fomq3w3)
Alternatively, use the QR code to access the same Doodle poll:

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Papers with identifiers ending in s have short presentations – 10 minutes – while papers with identifiers ending in p have posters only. All other papers have 20 minutes dedicated for presentation.